CLAIMS

What is claimed is:

1. An input stage circuit for an LVDS circuit comprising:

a folded cascode having a first input circuit and a second input circuit wherein said first input circuit receives a first input signal from a connected circuit and said second input circuit receives a second signal from said connected circuit;

a first current mirror that receives signals from said first input circuit of said folded cascode;

a second current mirror that receives signals from said second input circuit and wherein said first current mirror and said second current mirror are connected to a common output to merge signals from said first and second input circuits; and

a diode for adjusting a voltage level of said signals to an output voltage.

2. The input stage of claim 1 wherein said first input circuit comprises:

a first transistor; and

a second transistor connected in parallel to said first transistor.

3. The input stage of claim 2 wherein said first and said second transistors are N-channel MOS transistors.

4. The input stage of claim 2 wherein said first and second transistors are P-channel MOS transistors.

5. The input stage of claim 2 wherein said first and said second transistors are thin gate transistors.

6. The input stage of claim 1 wherein said second input circuit comprises:

a third transistor; and

a fourth transistor connected in parallel to said first transistor.

7. The input stage of claim 6 wherein said third and said fourth transistors are N-channel MOS transistors.

8. The input stage of claim 6 wherein said third and said fourth transistors are P-channel MOS transistors.

9. The input stage of claim 6 wherein said third and said fourth transistors are thin gate transistors.

10. The input stage of claim 6 wherein said third and said fourth transistors are of a different type than a type of a first and a second transistors in said first input.

11. The input stage of claim 1 further comprising:

at least one transistor in said first current mirror, wherein said at least one transistor is a thin gate transistor; and

at least one transistor in said second current mirror wherein said at least one transistor is a thin gate transistor.

12. The input stage of claim 1 wherein said diode comprises:

a first transistor having a source connected to a first source of said first input circuit and a drain connected to said output; and

a second transistor having a source connected to a second source of said first input and a drain connected to said output.

13. The input stage of claim 12 wherein said first and said second transistors in said diode are thin gate transistors.

14. The input stage of claim 1 further comprising:

a diode connected between said output and ground.

15. The input stage of claim 14 wherein said diode connected between said output comprises:

a transistor having a source connected to said output and a drain connected to ground.

16. The input stage of claim 15 wherein said transistor of said diode connected between said output and ground is a thin gate transistor.

17. An method for providing an input stage circuit for an LVDS circuit comprising:

applying signals to a folded cascode having a first input circuit and a second input circuit wherein said first input circuit receives a first input signal from a connected circuit and said second input circuit receives a second signal from said connected circuit;

applying output signals from said first output circuit to a first current mirror that receives signals from said first input circuit of said folded cascode;

applying output signals from said second input circuit to a second current mirror that receives signals from said second input circuit;

merging output signals from said first current mirror and said second current mirror; and

adjusting a voltage level of said signals to an output voltage though a diode connected between an input of said folded cascode and said output.